COMPREHENSIVE MODEL OF MICROWAVE FET ELECTRO-THERMAL AND TRAPPING DYNAMICS

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ABSTRACT

This paper presents a comprehensive model of microwave field-effect transistors aimed at describing the dynamic effects known to produce intermodulation asymmetry and frequency dispersion. It includes a first-time combination of accurate heating and trapping and impact-ionization descriptions in one model. The proposed architecture for the transistor is a static nonlinear drain-current model that is controlled terminal potentials and state variables of temperature and trap potential. All aspects of the model consider temperature. The channel temperature is determined by feeding the instantaneous power dissipation into a temperature node that is loaded by a thermal network. This network describes the heat capacity and thermal resistance of the path to ambient. A trap-centre model describes the bias dependence of trap potentials and the trapping rates. A trap centre is incorporated with a charging mechanism due to impact ionization. The model successfully predicts dc characteristics and transient behaviour. It also demonstrates potential to predict breakdown of the gate junction and the channel. The full model has been implemented in both time-domain and harmonic-balance simulators and provides stable and rapid simulations. It provides a comprehensive platform for the exploration of FET dynamics and large-signal nonlinearity.

INTRODUCTION

Heating and carrier-trapping effects generate complicated behaviour in microwave field-effect transistors that significantly influence their radio-frequency performance. The effects are known to produce intermodulation asymmetry, frequency dispersion, and memory effects, and cause the characteristics of FETs to change with the operating bias and frequency. The variations are dramatic enough that even the notional *dc* characteristics can vary with the timing and order of their measurement. A large-signal nonlinear model needs to be able to dynamically adapt to the varying bias conditions imposed by the circuit. Variation of temperature with power dissipation, which reduces drain current and intrinsic gain, is an important phenomenon. There are memory effects generated by charge trapping that shifts bias points and cause kinks in the characteristics that are frequency dependent. There are also breakdown phenomena. All these effects are strongly dependent on temperature.

A model of the memory effects has been presented, which identifies trapping and heating nonlinearities and their time constants as feedback mechanisms that affect broadband nonlinearity.[1] The precise architecture and accurate descriptions of each feedback element were identified as needing further investigation, however. Thus previous models provided only *proof of concept* simulations of the effects involved.[2]

An advancement to the models of the feedback elements is presented here as a foundation for future characterization and modelling work. The elements include elegant descriptions of trap centres, impact ionization, and heating that can be robustly implemented in circuit simulators. These descriptions are based on well-established physics. With these advancements, a detailed simulation of a comprehensive set of dynamic effects can be accomplished. The significantly-increased degree of freedom poses the problem of extracting parameters and composition of the model. However, the model presented here is suitable for investigating this.

The assembly of dynamic elements into a full model is also presented. The structure of the model allows control of individual elements, so that simulations can be performed to gain insight into the effect of each on transistor

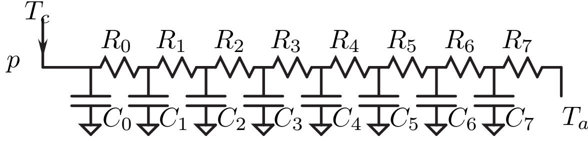


Fig. 1. Distributed thermal path from the transistor channel at temperature T_c to ambient at T_a, which are modelled by voltages at those nodes. A current p proportional to the power dissipation of the channel models the heat flow.

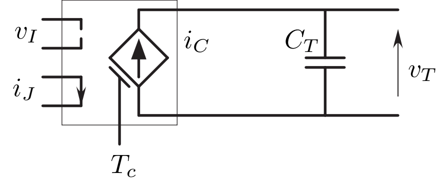


Fig. 2. Generic model of a semiconductor trap centre. The ionization potential of the trap v_T is developed across the capacitor. The nonlinear charging current is a function of temperature T, a control potential V_I, and injected current i_J.

characteristics. Two state variables have been found to be sufficient to allow simulation of isodynamic (instantaneous) large-signal characteristics for any bias point. These are total trap potential and temperature, which control a static nonlinear description of drain current. In addition, temperature dependence is applied to the gate-junction current and its breakdown.

The next Section presents details of the thermal and trap-centre networks. It also provides a first-time presentation of a full implementation of impact ionization within a transistor model. Then simulation examples including transient and small-signal results are presented. The simulations show the behaviour of the trap potential and temperature state variables, which provides insight into the operation of the transistor. Finally, the problem of parameter extraction is briefly addressed.

COMPREHENSIVE DYNAMIC MODEL

The comprehensive dynamic model of a microwave FET presented here is obtained when temperature variation with power dissipation, memory due to trapping, and impact ionization are accounted for. Each of these can be simulated by equivalent circuit modules, which are described in the following.

Channel Temperature

In an electro-thermal analogue, a representation of temperature can be voltage and of heat can be current. In this case, electrical resistance and capacitance are analogous to thermal resistance and heat capacity respectively. An equivalent-circuit model of the thermal path from the transistor channel to ambient is shown in Fig. 1. This is a ladder network in which the component values increase geometrically as they approach the ambient node. For the eight-element network in this example, the component values are:

$$R_i = \frac{a-1}{a^8-1}\, R_T\, a^i \tag{1}$$

and

$$C_i = \frac{f_c}{f_o}\,\frac{1}{R_i}\,\left[\frac{a^8-1}{25\, f_c\, a^7\,(a^7-1)}\right]^{i/7}, \tag{2}$$

where R_T [$\Omega \equiv$ K/W] is the total thermal resistance from the channel to ambient, $1/f_o$ is the thermal time constant, $a = (n+1)/(1-n)$ where n is the order of the thermal response, which is approximately 0.3 to 0.5 typically, and f_c is the cut-off frequency for the network (typically a few GHz).[3] The factor of 25 improves the approximation to an ideal n^{th}-order response for typical values of n. It would vary if other than eight elements were used.

When implemented in a simulator model, the network is attached to a voltage source equal to the ambient temperature T_a and driven by a current p, which is proportional to the power dissipation of the channel. The voltage at the driven node will be equal to the channel temperature. In practice, setting this to 1 V/°C gives a sensible starting point if the simulator uses an initial guess of zero. An extraction procedure for the heating parameters is given in [3].

Trap Model

Within the structure of microwave transistors there are regions of semiconductor that trap charge in mid-band energy states.[4] The extent and period of trapping is well described as capture and recombination processes.[5] In a transistor, the trap centres cause memory effects with bias and frequency dependence that significantly affect its dynamics and nonlinearity.[6], [7], [8]

A generic trap-centre model has been developed for transistor circuit simulators, which implements trapping by storing charge in a capacitance C_T [F] that is fed by a nonlinear controlled-current source as shown in Fig. 2.[9],[10] The potential across the capacitor v_T is the trap's ionization potential and charge within it is proportional to the charge in the trap. The current source is the sum of recombination and capture rates, which are functions of temperature T [K] (and the Boltzman constant k [eV/K]), given by

$$i_C(v_T, v_I, i_J, T) = \omega_o(T)\, C_T \left[V_O - v_T - v_T\, \alpha_T(i_J)\, \exp\left(\frac{v_I}{kT}\right)\right], \tag{3}$$

where V_O is the potential of trap when it is fully ionized,

$$\omega_o(T) = A_T\, T^2\, \exp\left(-\frac{E_T}{kT}\right) \tag{4}$$

is the trap's emission rate in terms of an Arrhenius factor $A_T\, T^2$ [s^{-1}] and activation energy E_T [eV], and

$$\alpha_T(i_J) = \begin{cases} 1 + C_J\, |i_J| & \text{if } i_J\, V_O \leq 0 \\ 1/(1 + C_J\, |i_J|) & \text{if } i_J\, V_O > 0 \end{cases} \tag{5}$$

is the *availability factor* of additional carriers for capture, which is a function of current i_J injected into the region and parameter C_J [A^{-1}].

The trap centre obtains neutral charge if it captures enough carriers to occupy all its states. A donor trap captures electrons while an acceptor trap captures holes. However, the trap emits carriers through thermal excitation, so the centre becomes ionized with a potential opposite to that of the captured carriers. Thus $V_O > 0$ for an electron trap formed by donor states and $V_O < 0$ for a hole trap formed by acceptor states.

When current of the correct polarity for capture is injected into the region, the capture rate is increased. Thus when V_O and i_J are of opposite polarity the injection current in (5) adds to the population of carries that can be captured and α_T increases. Otherwise the injected current acts to deplete the intrinsic concentration of carriers available for capture.

In the steady state, the trap potential is

$$V_T(V_I, I_J, T) = \frac{V_O}{1 + \alpha_T(I_J)\, \exp\left(\frac{V_I}{kT}\right)} \tag{6}$$

and the characteristic frequency for the trapping process is

$$\omega(V_I, I_J, T) = A_T\, T^2\, \exp\left(-\frac{E_T}{kT}\right)\left[1 + \alpha_T(I_J)\, \exp\left(\frac{V_I}{kT}\right)\right], \tag{7}$$

where V_O, A_T, E_T, and C_J completely parameterize the trap centre.

Impact Ionization

When the drain-source potential produces sufficient lateral electric field, high-velocity electrons cause impact ionization. The rate of impact ionization is generally of the form $A \exp(-B/(V_{DS} - V_{SAT}))$ with parameters A, B [V], and parameter V_{SAT} [V], which is the critical drain-source potential required to cause impact ionization.[11]

A practical implementation of the impact-ionization rate that is proposed here is given by

$$R_I(v_{DS}, T) = \left[\exp\left(\frac{B\,(1 + \lambda_B\, T)}{\sigma_I\, E_I(v_{DS})} - \frac{\ln(A)}{\sigma_I}\right) + 1\right]^{-\sigma_I}, \tag{8}$$

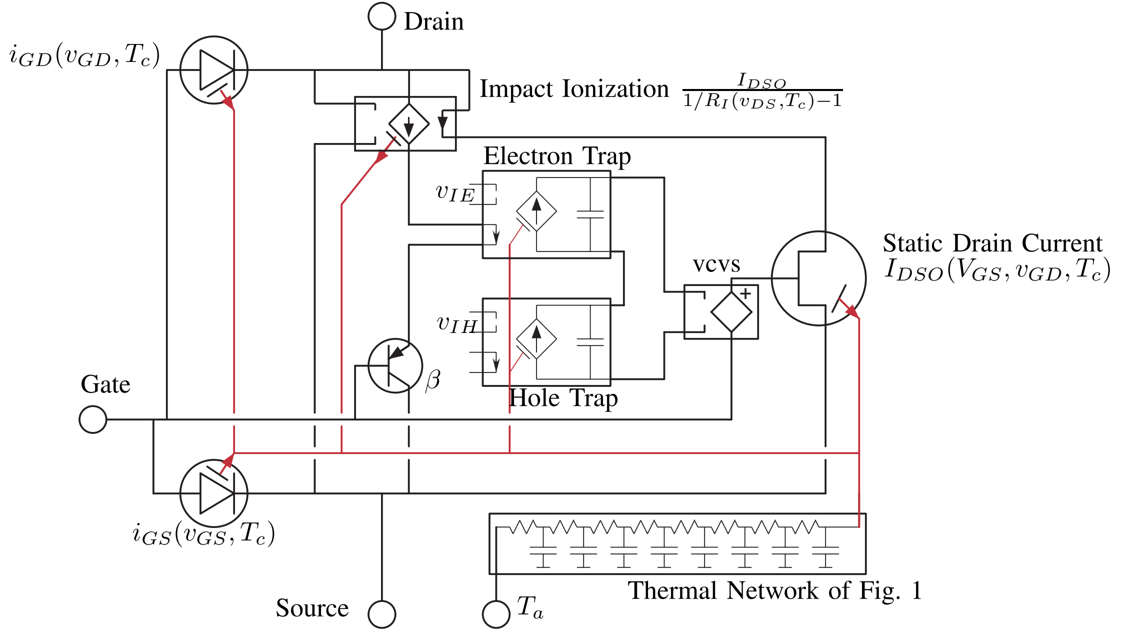


Fig. 3. The comprehensive FET model, which generates states variables of temperature and total trap potential to control a static drain-current element. Impact ionization current is divided between gate and source currents by an ideal BJT element. Gate-junction current and breakdown are implemented by temperature dependent diode elements.

where E_I is the electric field strength calculated as

$$E_I(v) = \frac{1}{2}\left[\sqrt{Z^2 + (v - V_{SAT})^2} + \sqrt{Z^2 + (v + V_{SAT})^2} - \left(2 - \frac{0.08\,B}{V_{SAT}}\right)\sqrt{Z^2 + V_{SAT}^2}\right], \tag{9}$$

which limits to a positive value greater than zero for either polarity of v_{DS} with smoothing parameter Z. The factor 0.08 prevents the field from reaching zero, which maintains a small impact-ionization rate to prevent numerical underflow. The parameter σ_I sets the width of the transition to impact ionization as v_{DS} varies from less than to greater than V_{SAT}.

The temperature coefficient of B is λ_B, which implements the observed reduction in impact ionization at higher temperatures.[12][13]

The additional drain current generated by impact ionization is $i_{DS}\,R_I$, so the total drain current is $i_{DS} = i_{DSO} + i_{DS}\,R_I$ where i_{DSO} is the drain-source current if impact ionization is not considered. This gives a net current of

$$i_{DS} = i_{DSO} + i_{DSO}\frac{R_I}{1 - R_I}, \tag{10}$$

which will break down as $R_I \rightarrow 1$. The second term is the additional electron current generated by impact ionization, which is balanced by a hole current injected into the gate and source regions of the transistor. It can be observed as an increase in gate current and also provides and injection current to surface traps.[6]

Model Implementation

A comprehensive dynamic model of a FET is shown in Fig. 3. It has four terminals; drain, gate, source, and temperature. The core of the model is a static drain-current element, which is an isodynamic function of terminal potentials, trap potentials, and temperature.[14],[3],[15] The main feature of this element is that it sources a current equal to its instantaneous power dissipation to its temperature node, which is connected to the thermal network of Fig. 1. This is analogous to heat flow from the current element through the thermal path to ambient.

The total drain current is the sum of the static and impact-ionization currents (10) and the gate-drain diode current. The latter sources its power-dissipation current to the temperature node and is temperature dependent.[4] A fraction

$1/\beta$ of the impact-ionization current is fed to the gate and the balance appears as source current. The schematic uses an ideal bipolar transistor to implement this.

In this example, which fits the device presented here, there is a hole trap and an electron trap that is fed by injected hole current from impact ionization. The traps are controlled by potentials v_{IE} and v_{IH} respectively, where

$$v_{IE} = k_e + k_{eg}\, v_{GS} + k_{ed}\, v_{DS} \tag{11}$$

and

$$v_{IH} = k_h + k_{hg}\, v_{GS} + k_{hd}\, v_{DS}. \tag{12}$$

In general, any combination or number of traps can be implemented to suit particular devices and processes. The sum of the ionization potential of these traps is added to the gate potential of the static drain-current element.

For the hole trap, $k_{hg} > 0$, which ionizes the trap to a more-negative potential as the transistor is pinched off by a negative gate potential, and $k_{hd} > 0$, which reduces the ionization as the drain potential is increased. This models the effect of electron injection toward the substrate reducing the ionization of the hole trap. This ionization of the trap when the transistor is pinched off is at the emission rate. When the transistor is turned on, there is a delay or gate lag while the trap captures holes at a capture rate that exponentially increases with v_{IH} and also with temperature. The dynamic for this, which is observed in pulse measurements, is that the gate lag is slower at lower drain potentials and that the time required in the off state is independent of bias.

For the electron trap, $k_{eg} < 0$, which ionizes the trap to a more-positive potential as the gate potential increases, and $k_{ed} > 0$, which reduces the ionization as the drain potential is increased. This models the effect of holes injected into the surface increasing the ionization of the electron trap. The trap is also ionized by hole current from impact ionization that generates the kink in the drain-current characteristics. This is included as an injection current feeding the trap-centre model. When the transistor is turned on at high drain potential, there is a gate lag while the injection current ionizes the traps at the emission rate. When the drain potential is subsequently reduced, the trap will capture holes at a rate that exponentially increases with v_{IE} and that also depends on temperature. The dynamic for this is that the formation of the kink in the characteristics is slower at lower drain potentials.

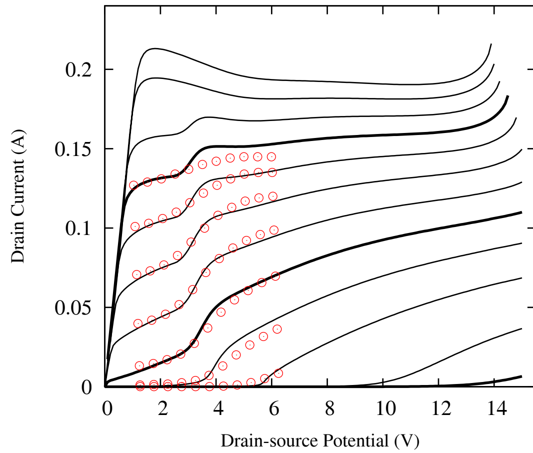
SIMULATIONS AND MEASUREMENTS

A simulation of a 0.2×250 μm pHEMT was carried out with the parameters given in Table I. The dc characteristics are shown in Fig. 4. There are several features in these characteristics that are worth noting. At high drain potential there is breakdown of the gate-drain diode junction. This occurs at lower potentials for higher power levels because of the higher temperature. That is, the diode-junction breakdown undergoes thermal runaway. (Impact-ionization induced breakdown, or avalanche breakdown in the channel, is reduced at higher temperatures.[12],[13] It is possible to simulate this form of breakdown by increasing A in (8). In this case the simulated breakdown is found to settle to a finite current — albeit at extreme temperatures.)

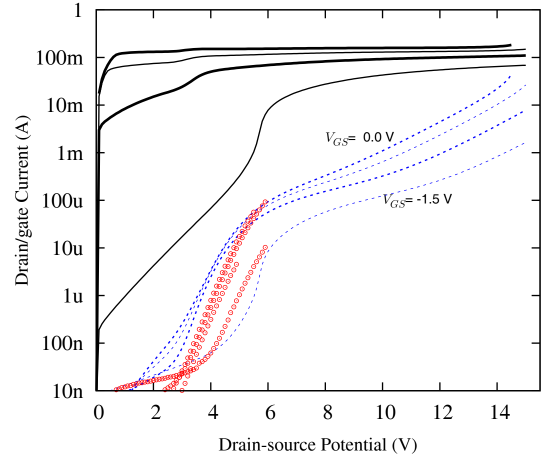
At around four volts, there is a kink due to the ionization potential of the electron trap, due to hole injection from impact ionization. There is a corresponding three orders-of-magnitude increase in gate current due to the hole current from impact ionization. The kink is observed at potentials lower than that at which gate current increases because of the greater effect of feedback through the electron trap. The corresponding trap-potential simulation is shown in Fig 5(a). This potential is positive when the electron trap is ionized and driven negative when the hole trap is ionized. For positive gate potentials, there is hole injection that fully ionizes the surface trap even when there is no impact ionization. Thus there is no kink in the top two curves of Fig. 4(a).

Figure 5(b) shows the simulated channel temperature as a function of bias. At low drain potentials there are kinks corresponding to those in the drain current. The high temperatures at high power and in the breakdown region are those predicted by the simulation. This is very useful as a design guide provided it is recognized that a real transistor may cease to function at these extremes.

A simulation of the transient response of drain current is shown in Fig. 6. The model predicts the response over several decades of time in both switch-on and switch-off directions. It describes a rich set of dynamics and exposes the

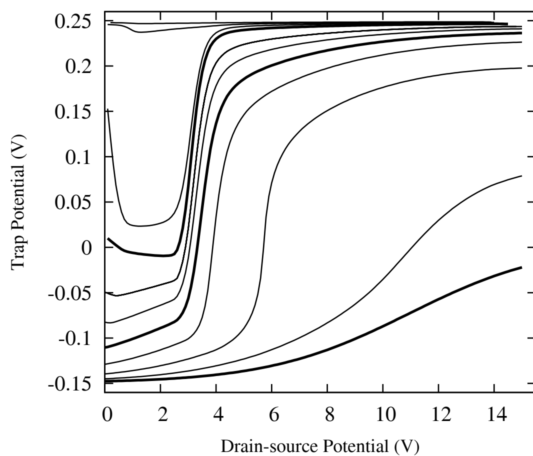


(a) Characteristics for gate-source potential from –2.0 V to +0.75 V in 0.25V steps as a parameter.

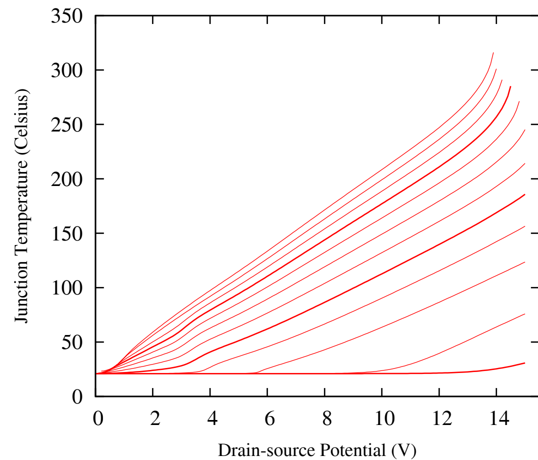


(b) For gate-source potential from –1.5 V to +0 V in 0.5V steps as a parameter. The drain current (—) is a subset of the data in Fig. 4(a) and the corresponding gate current (- -) shows clear evidence of impact ionization.

Fig. 4. Simulation of dc characteristics of a $0.2 \times 250\ \mu$m pHEMT. The points (○) show measurements for comparison.



(a)



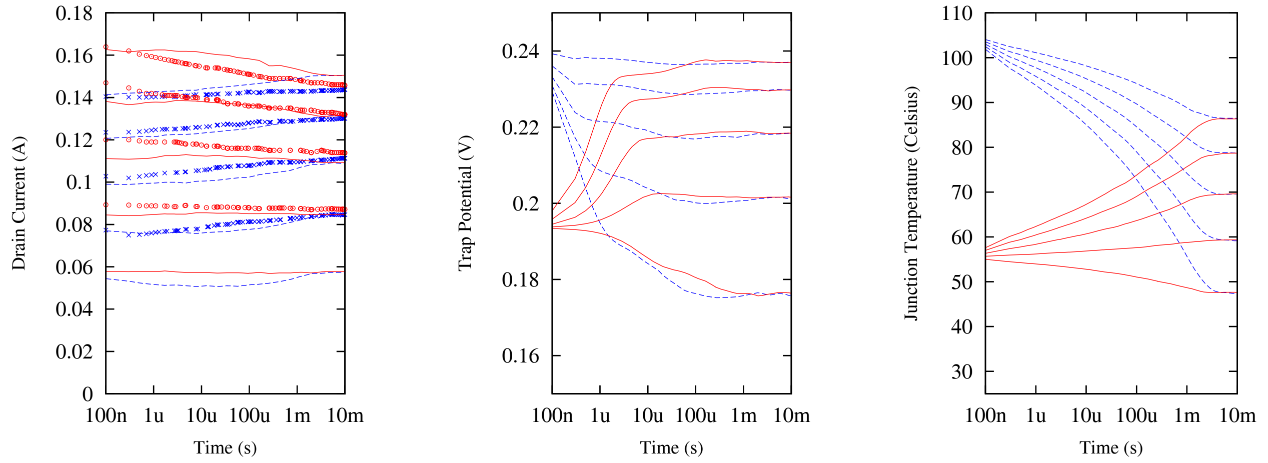
(b)

Fig. 5. Simulation of trap potential and temperature of a pHEMT for gate-source potential from –2.0 V (bottom curve) to +0.75 V (top curve) in 0.25V steps as a parameter. The data corresponds to the characteristics of Fig. 4.

processes of trapping and heating as they occur during stages of the transient. This is a very useful aid for exploring the operation of the transistor. Figs 6(b) and 6(c) illustrate the variation of trap potential and temperature that occurs at varying time points. This variation and its rate depend on the bias and, for the traps, on temperature. It can been seen that the ionization of surface traps during turn-on is faster than the emission that occurs during switch-off. This is because the latter simulation occurs at a higher temperature.

Note that the results were obtained with no optimization or explicit fitting of parameters. Rather, the model was fitted to the dc data of Fig 4. There are more than sufficient degrees of freedom for accuracy but this presents a challenging fitting task that requires additional information such as offered by intermodulation and small-signal RF measurements. The model presented here is a platform with sufficient detail for a fuller investigation of this.

Intermodulation and small-signal RF simulations are shown in Fig. 7. This illustrates the rich variation of the RF characteristics of HEMTs over frequency and the effect of memory on nonlinearity that is observed in real devices.[1], [2] The intrinsic gain of Fig. 7(a) shows significant reduction at the onset of impact ionization, which extends up to

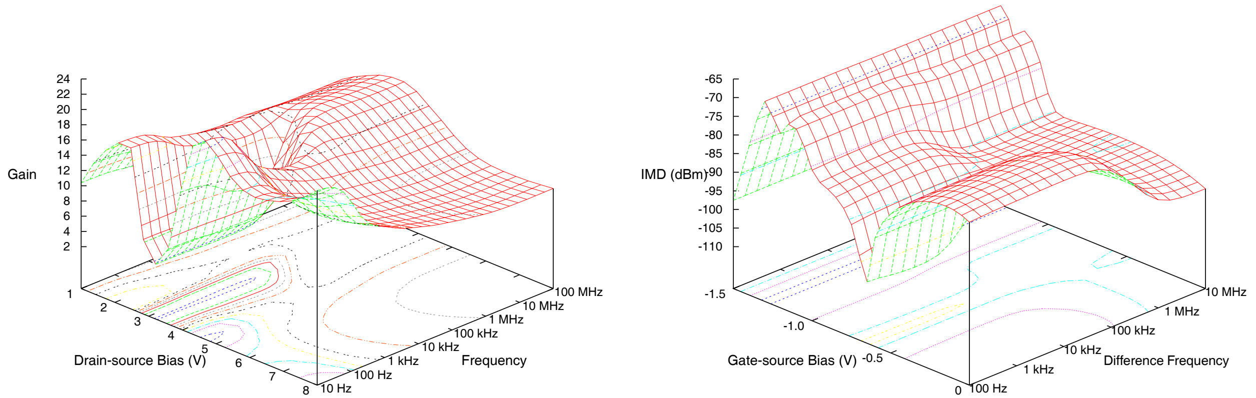


(a) Drain current simulation (lines) and measurement (points)

(b) Trap potential from simulation.

(c) Channel temperature from simulation.

Fig. 6. Simulation of transient response after a step change to gate-source potentials of –1.00, –0.75, –0.50, –0.25, and 0.00 volts from initial biases of $V_{GS} = 0$ (- -) and $V_{GS} = -1.0$ (–). In all cases the drain potential is simultaneously stepped down from 6.0 V to 4.5 V.



(a) Intrinsic gain (y_{21}/y_{22}) at $V_{GS} = -0.5$ V.

(b) Two-tone intermodulation level at $V_{DS} = 3.0$ V versus tone spacing for a centre frequency of 1 GHz.

Fig. 7. Simulation of the intrinsic gain and intermodulation product for a pHEMT.

the frequency corresponding to the capture/emission rate of the electron trap. At high drain potential there is a boost in gain at low frequencies due to the positive-feedback effect of heating. Minor variations in the trapping parameters can significantly alter the structure of the intrinsic gain surface, so it can be used as a basis for extracting model parameters.

The intermodulation surface of Fig. 7(b) shows the effect of memory due to trapping and heating on the nonlinearity of the transistor. This surface shows the vector sum of static nonlinearity and the nonlinear feedback of difference-frequency components present in the trap potential and temperature node.[16] The increase in intermodulation at zero gate bias / low frequency (front corner of the figure) is affected by the electron trap. The frequency at which the intermodulation level drops varies exponentially with drain bias and can be controlled by the impact-ionization parameters. The phase of the trap potential will be such that it will either add to or subtract from the intermodulation. As this is linked to the polarity of the trap, the intermodulation surface can provide further insight into the nature of the corresponding parameters.

MODEL EXTRACTION

The simulations shown above illustrate the rich dynamic behaviour that the model can reproduce. These extend over orders of magnitude in time and frequency. Measurement of real transistors reveals the same behaviour extending over similar time and frequency scales. Bias and temperature dependence is also significant in both the simulations and measurements.

A significant degree of freedom is offered by the choice of number of traps and the choice of trap, heating, impact-ionization, and breakdown parameters. The complexity of fitting the model to measurements is challenging and remains a continuing area of investigation. It is clear that many vectors of measurement, such as small-signal frequency-domain, pulse time-domain, and temperature-domain, are required to identify the dynamic elements in a specific device.

CONCLUSION

A comprehensive model of a HEMT has been presented for the simulation of heating and trapping-related dynamics of the transistor. The key elements of the model are descriptions of temperature, trapping, impact ionization, and gate-junction conduction that have been combined into a total dynamic system. This has been facilitated by the development of practical implementations of trap centres, the impact-ionization process, and the thermal path. These are accurate over a wide range of conditions and are a significant advancement over single-pole networks that are often used for delineating dc and ac characteristics.

The ensemble of phenomena in the model offers the ability to study and explore the dynamics of FETs in detail. The introduction of the two state variables proposed here facilitates this. This work also paves the way to a comprehensive characterization of memory-related mechanisms and large-signal nonlinearity. The model is applicable over the entire baseband, which is important for wide-band communications applications.

ACKNOWLEDGEMENTS

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TABLE I
PARAMETERS USED IN THE SIMULATIONS.

PARAMETER	VALUE	UNITS	PARAMETER	VALUE	UNITS
R_T	100.0	K/W	B	3.0	V/V
f_o	100.0	Hz	V_{SAT}	4.0	V
f_c	10.0	GHz	λ_B	5.0	mV/VK
n	0.2		Z	2.0	V
T_a	21.0	°C	β	100	A/A
E_T	0.5	eV	k_h	50.0	mV
A_T/T^2 for h trap	86.4	MHzK^2	k_{hg}	80.0	mV/V
V_O for h trap	–150.0	mV	k_{hd}	10.0	mV/V
A_T/T^2 for e trap	8.64	MHzK^2	k_e	50.0	mV
V_O for e trap	250.0	mV	k_{eg}	–40.0	mV/V
C_J for e trap	5.0	V/μA	k_{ed}	50.0	mV/V
A	500.0	mA/A			

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